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01_Revision_History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1	RC00	2018-12	GW	- Bugfix	
2.0	RC00	2020-11	GF	- New sensing stucture; new TDSO footprint; bugfixes	
2.1	RC00	2021-03	GF	- GND layer removed, satellite sensor configuration	
2.2	RC00	2021-07	GF	- Restored GND layer for better dI/dt immunity	
2.3	RC00	2021-10	GF	- Introduced LDO for better supply stability.	

TLE4972 TDSO16 InlayPCB S-Bend Evaluation Board

Default_Assembly

2.3

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10/2021

Link to Top Level Document

02 Top Level
02_Top_Level.SchDoc

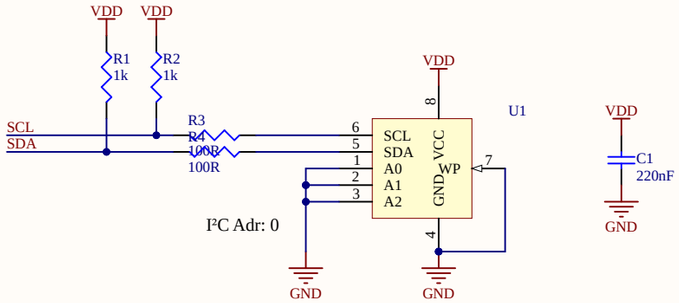
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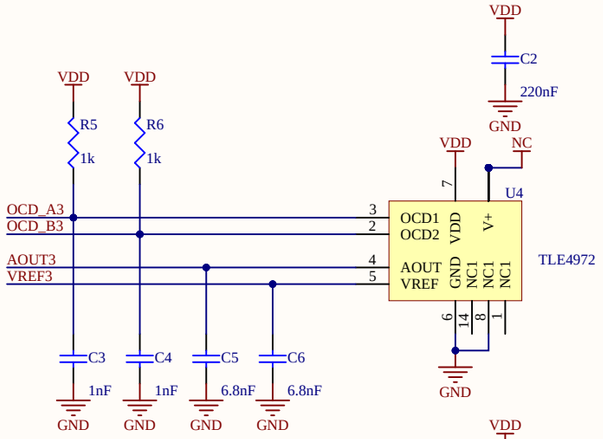
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Date: 12.10.2021 Time: 08:31:47	Author: GF	Sheet	of 3

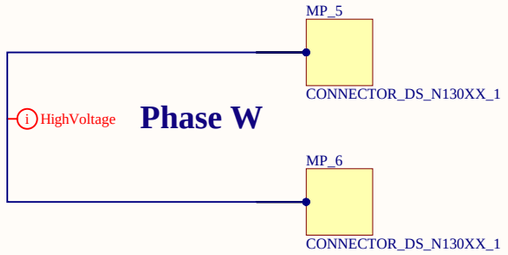
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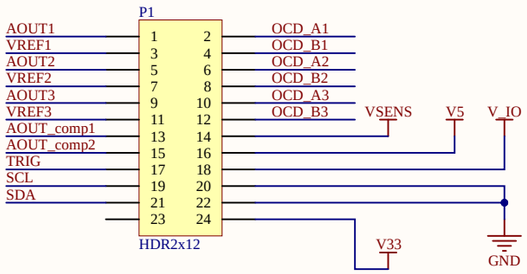
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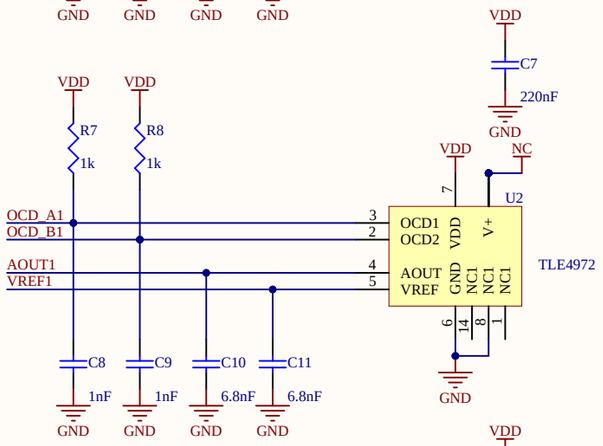


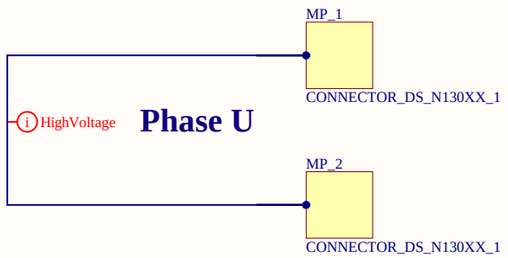


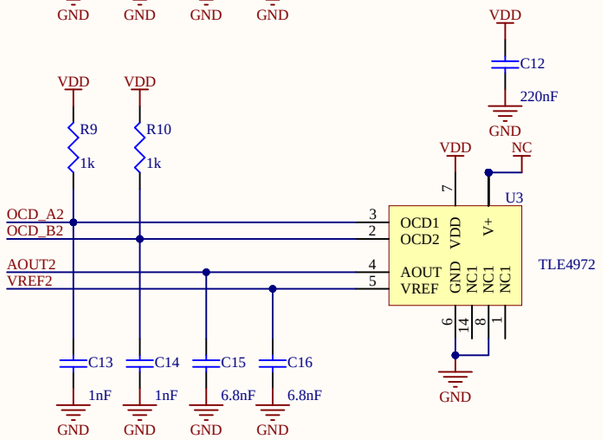


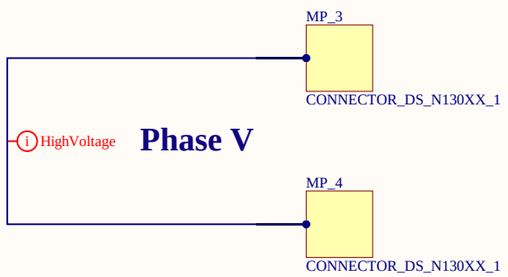
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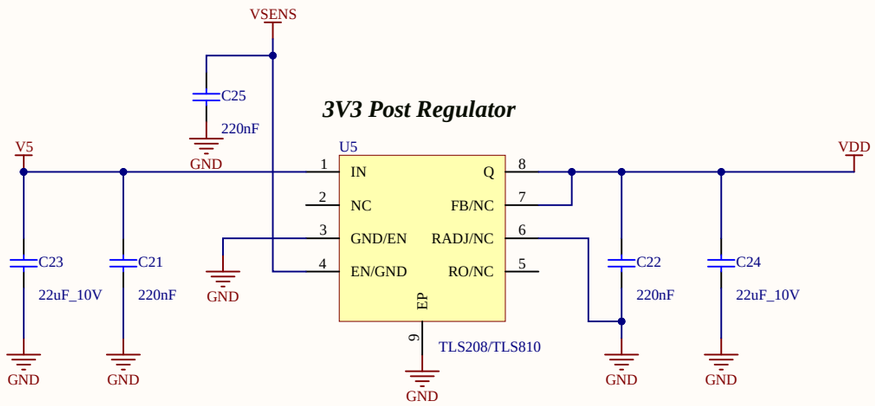
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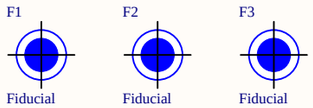
Miscellaneous
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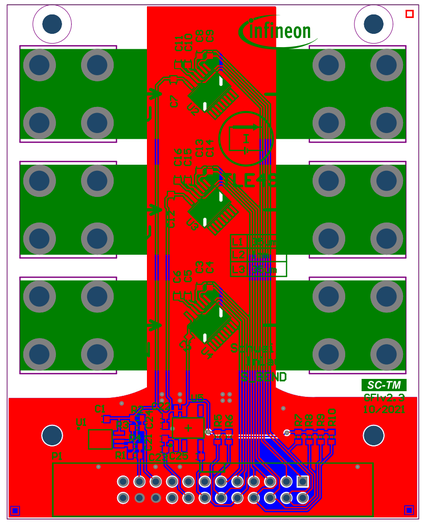
BOM Report Configuration

Note!
This component is used to define BOM report configuration.
If this component is deleted before other components from database are placed in this project, the BOM report configuration gets lost!

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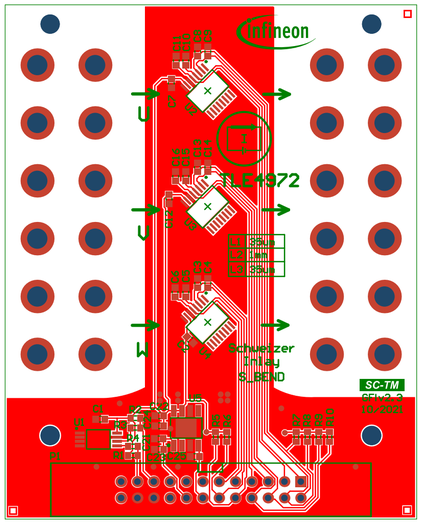


Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.030mm	3.5	
	galv. Cu top		0.043mm		
1	L1_Top	copper	0.032mm		
	Prepreg1	FR4	0.050mm	4.6	
	Prepreg2	FR4	0.050mm	4.6	
2	Inlay	copper	1.000mm		
	Prepreg3	FR4	0.050mm	4.6	
	Prepreg4	FR4	0.050mm	4.6	
3	L3_Bottom	copper	0.032mm		
	galv. Cu bottom		0.043mm		
	Bottom Solder	Solder Resist	0.030mm	3.5	
	Bottom Overlay				

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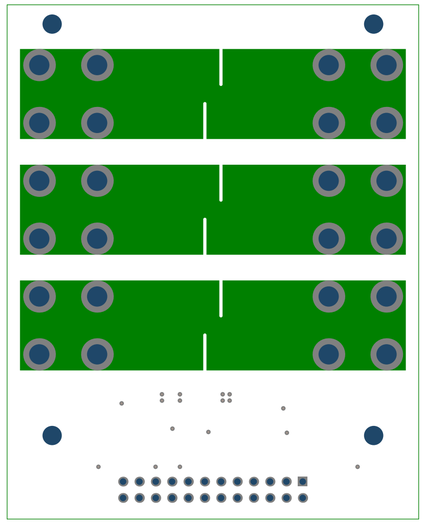
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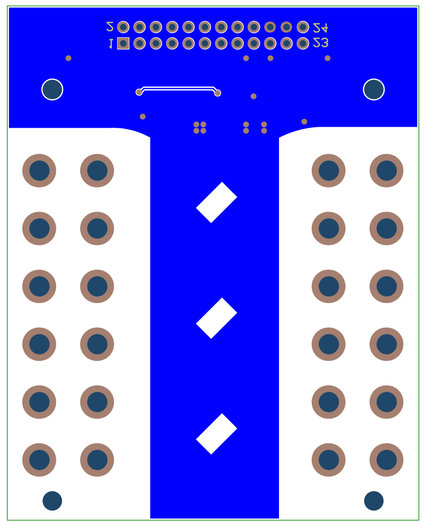
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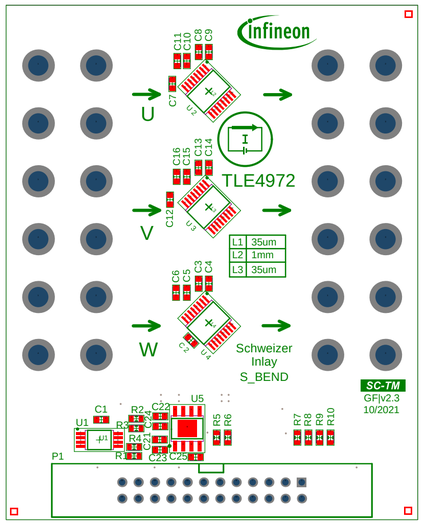




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ENGINEER:				

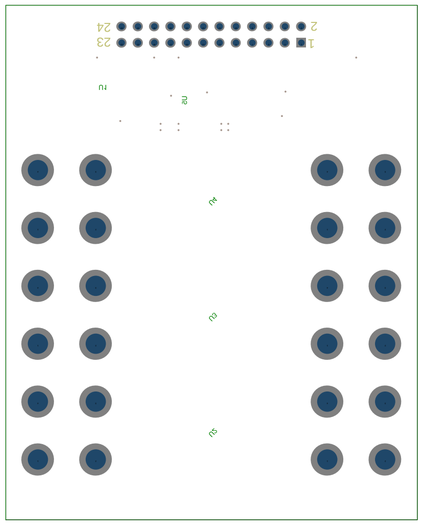
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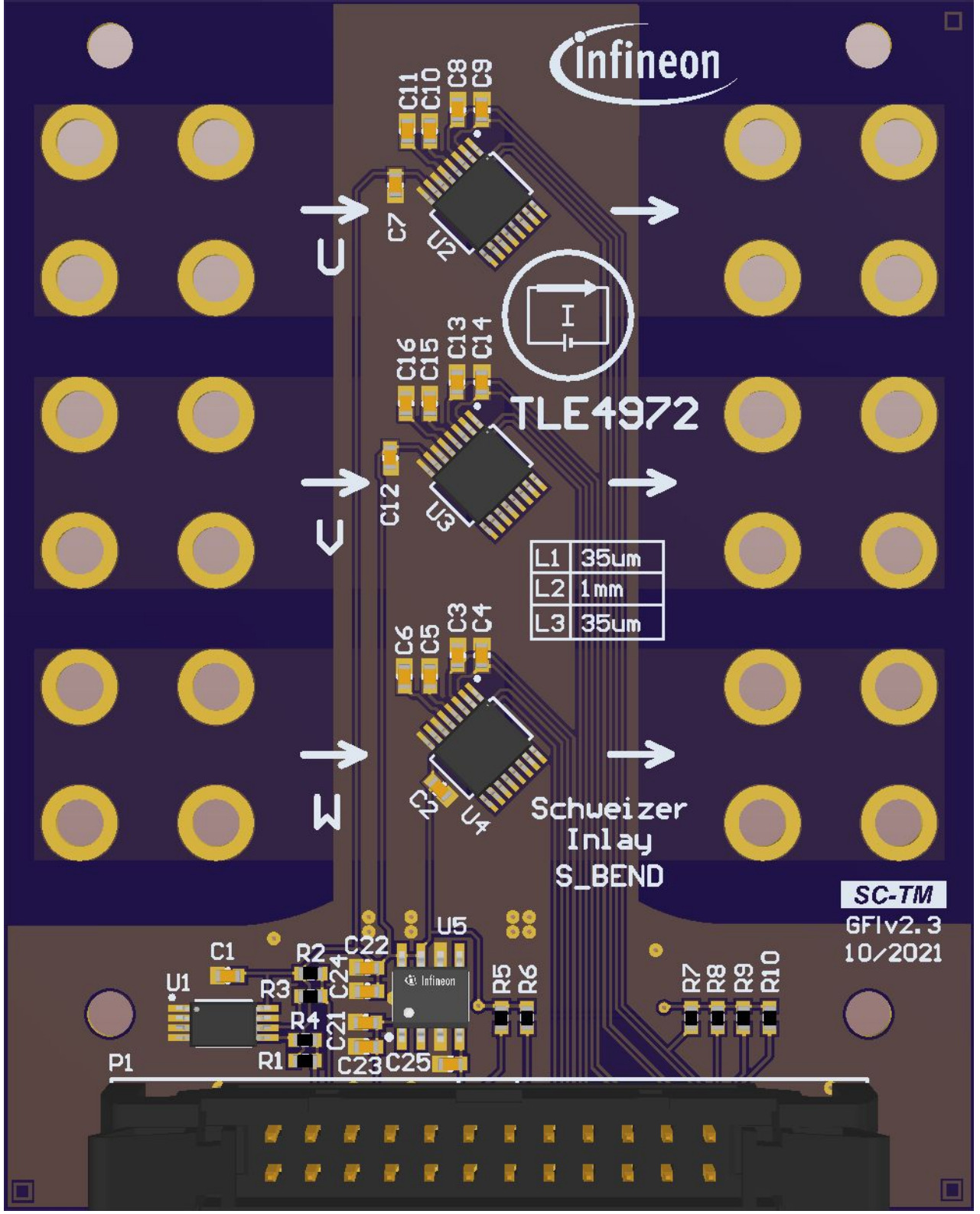
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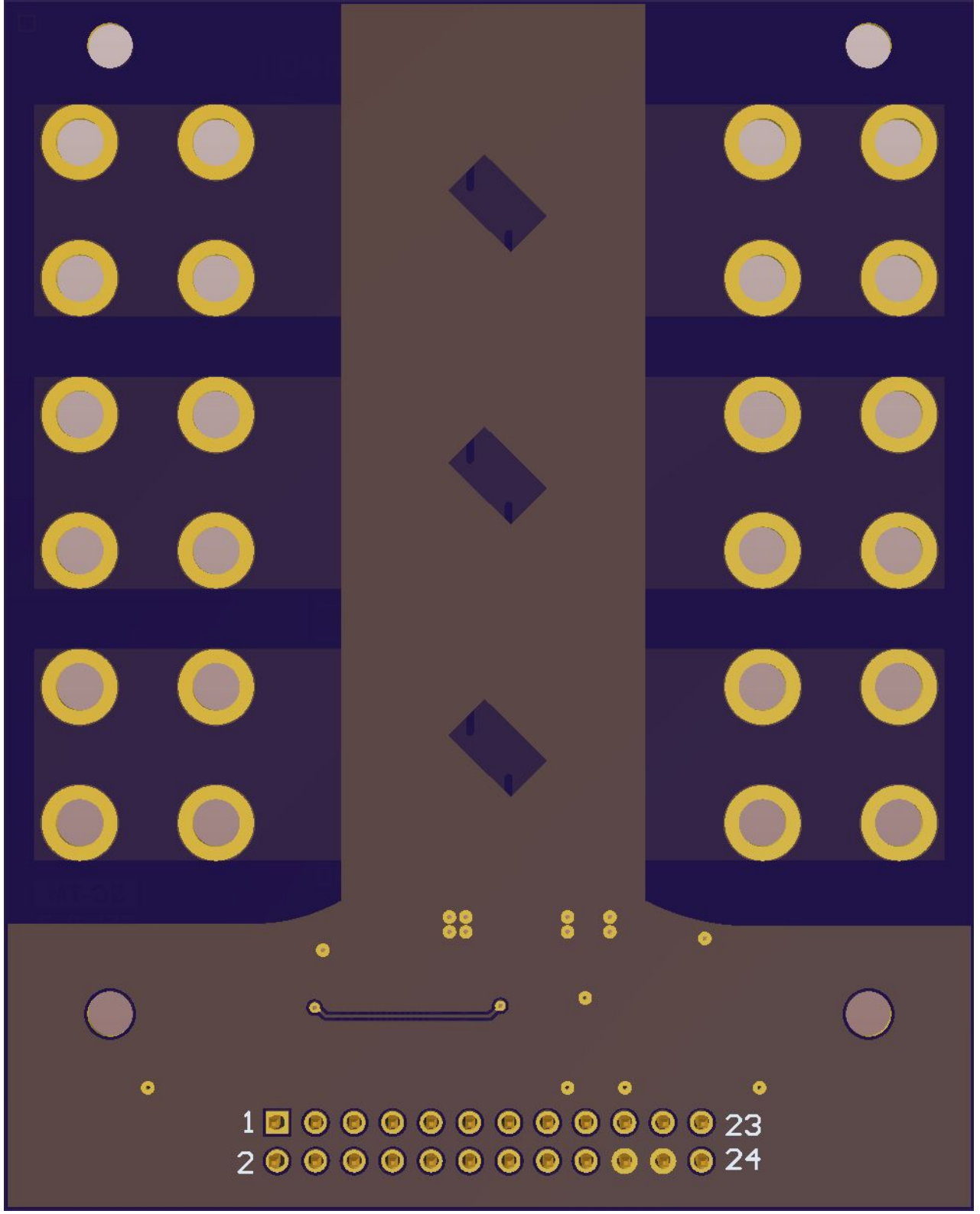


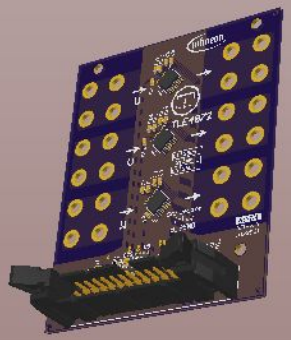
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Infineon
TLE4972
L1 35um
L2 1mm
L3 35um
Schweizer
Inlay
S_BEND
SC-TM
GFIv2.3
10/2021
U1
U2
U3
U4
U5
P1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
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R1
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R3
R4
R5
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R10


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23
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24


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